College of Engineering & Technology					
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Question Bank					
Year/Semester:	Department	: AI&DS	Unit	: II, IV,V	
II/ III Subje	Subject Code/Ti	tle : CS3351/ DIGITAL PRINCIPLES	Section	: Part A/B/C	
Date: 8.11.2024		AND COMPUTER ORGANIZATION			
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UNIT-II-SYNCHRONOUS SEQUENTIAL LOGIC

Part A:

1. What is a ring counter?

A ring counter is one, in which a single '1' is made to circulate around the register. An'n' bit ring counter has 'n' states.

2. Write short notes on propagation delay.

Propagation delay symbolized t_{pd} is the time required for a digital signal to travel from the input of the logic gate to the output. It is measured in microseconds, nanoseconds or picoseconds.

3. Discuss the working of T flip-flop.

- T flip-flop is also known as Toggle flip-flop.
- When T=0 there is no change in the output.
- When T=1 the output switch to the complement state (ie) the output toggles.

4. What is the operation of JK flip-flop?

The operation of JK flip-flop is as

- When K input is low and J input is high the Q output of flip-flop is set.
- When K input is high and J input is low the Q output of flip-flop is reset.
- When both the inputs K and J are low the output does not change
- When both the inputs K and J are high it is possible to set or reset the flip-flop (i.e.) the output toggle on the next positive clock edge.

5. What are the significances of state assignment?

Static assignment is assigning binary values to states that will create a reduced logic equation.

6. Write any two applications of shift register.

The applications of shift register are as

- Serial to parallel converter
- Parallel to serial converter
- As a counter
- To introduce delay in a digital circuit

7. How does synchronous circuit differ from asynchronous circuit?

Asynchronous circuits	Synchronous circuits
The output of the first flip-flop drives simultaneously.	All the flip-flops are clocked the clock for next flip-flop.
They are slow, because the clock is propagated through number of flip-flops before it reaches last flip flop.	As clock is simultaneously given to all flip-flops there is no problem of propagation delay.
Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of states increases.

8. What is the drawback of SR flip-flop? How it is avoided in JK flip-flop? [A/M -18]

In SR flip-flop, when both inputs are 1, the output Q and Q' will be equal. So this is indeterminate state. In JK flip-flop, another feedback is given from output in input side, so the output will be complement of the previous state, if the inputs are '1'.

9. List out the different types of shift registers.

The different types of shift registers are:

- Serial In Serial Out (SISO) shift register
- Serial In Parallel Out (SIPO) shift register
- Parallel In Serial Out shift register
- Parallel In Parallel Out shift register.

10. What are synchronous sequential circuits?

Synchronous sequential circuits are those in which signal can affect the memory element only at discrete instants of time. Clocked flip-flops are examples of synchronous sequential circuits.

11. Define – Sequential Logic Circuit. Write an example. [May/June – 08]

The circuits in which the output variables depend not only on the present input but they also depend upon the past outputs, which are known as sequential logic circuits. Flip-flops, counters and registers are the examples of sequential logic circuit.

12. Draw the logic diagram of SR flip-flop.



13. What are the classifications of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are,

- Synchronous sequential circuit.
- Asynchronous sequential circuit.

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14. Define Flip flop.

Flip flop is defined as a digital circuit which maintains its output state either at 1 or 0until directed

by an input signal to change its state. (Or)

Flip - flop is a sequential device that normally samples its inputs and changes its outputs only at times determined by clocking signal.

15. Give the comparison between combinational circuits and sequential circuits.

Combinational circuits	Sequential circuits
Memory unit is not required.	Memory unit is required.
Parallel adder is a combinational circuit.	Serial adder is a sequential circuit.

16. What is meant by present state?

The information stored in the memory elements at any given time defines the present state of the sequential circuit.

17. What is meant by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

18. What are shift registers?

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

19. What is a master-slave flip-flop?

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

20. What is the operation of SR flip-flop?

- When R input is low and S input is high the Q output of flip-flop is Set.
- When R input is high and S input is low the Q output of flip-flop is Reset.
- When both the inputs R and S are low the output does not change.
- When both the inputs R and S are high the output is unpredictable.

21. Compare asynchronous and synchronous sequential circuit.

Sl.No	Synchronous sequential circuit	Asynchronous sequential circuit	
L	Memory elements are clocked flip- flops.	Memory elements are either un- clocked flip-flops or time delay elements.	
2	The change in input signals can affect memory element upon activation of clock signal.	The change in input signals can affect memory element at any instant of time.	
3	It is slower.	It is faster.	
4	It is easier to design.	It is more difficult to design.	

22. What is edge triggered flip-flop?

• If the flip-flop changes its state when the clock is positive(High) or negative(Low) then, that flip-flop is said to be level triggering flip-flop.

• If the flip-flop changes its state either at the positive edge (rising edge) or negative edge (falling edge) of the clock and is sensitive to its inputs only at this transition of the clock then that flip-flop is said to be edge triggered flip-flop.

23. Define - Race Around Condition

In JK flip- flop, if both J and K are high and when clock is also 1, then the output toggles continuously between set and reset state. This condition is known as race around condition.

24. List the various memory elements used in sequential machines.

The various memory elements used in sequential machines are D flip-flop, T flip-flop, SR flip- flop, and J-K flip-flop.

25. What do you mean by the term 'state table'? What does each row, column and entry of the state table represent?

The state table is a tabular representation of the relationship between the present state, the input, the next state and the output. Each column of the state table corresponds to one input symbol, and each row of the state table corresponds to one state. The entries corresponding to each combination of the input symbols and the present state specify the output that will be generated and the next state to which the machine will go.

<u>Part B:</u>

- 1. A) Explain the Logic diagram & Truth table of JK flip-flop?
- B) Write difference between Combinational & Sequential circuits?
- 2. A) Explain the Logic diagram & Truth table of SR flip-flop?
- B) Design and draw the 3 bit up-down synchronous counter?
- 3. A) Draw and explain the operation of D Flip-Flop?
- B) Explain about Shift registers?
- 4. A) Draw and explain the operation of SR LATCH?
- B) Explain about Ring counter?
- 5. A) Explain about ripple counter?
- B) What is state assignment? Explain with a suitable example?
- 6. Explain the design of a 4 bit binary counter with parallel load in detail ?
- 7. How does it set eliminate is a Master --slaves J-K flip flop?
- 8. A) Explain synchronous and ripple counters compare their merits and demerits?
- B) Design a 4 bit binary synchronous counters with D-flip flop?
- 9. A) Write the truth table of clocked T-Flip Flop?
- B) Define shift registers?
- C) Write the differences between latches and flip flops?
- D) Write the differences between synchronous and asynchronous counters?
- E) Define Flip-Flop and various types of flip flops?
- 10. Design a synchronous counter with the following sequence: 0,1,3,7,6,4 and repeats.
- 11. Using D flip flops, design a synchronous counter which counts in the sequence,
- 000, 001, 010, 011, 100, 101, 110, 111, 000
- 12. (i) Design a shift register using JK flip flops
- (ii) Explain the difference between a state table, characteristics table and an excitation table
- 13. (i) How race condition can be avoided in a flip flops?
- (ii) Realize the sequential circuit for the state diagram shown below.
- 14. Design a synchronous counter that counts the sequence 000, 001, 010, 011, 100, 101, 110, 111, 000

using D flip flop

- 15. Implement T flipflop using T flipflop and JK flipflop using D flipflop.
- 16. Design a binary counter using T flip flops to count in the following sequences:
- (i) 000, 001,010,011,100,101, 111, 000
- (ii) 000, 100, 111, 010, 000
- 17. Design three bit synchronous counter with T flipflop and draw the diagram.
- 18. Design a sequence detector that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line and produces an output whenever this sequence is detected.

Part C:

- 1. Desgin a modulo 5 synchronous counter using JK Flip Flop and implement it. Construct its timing diagram.
- 2. Design synchronous mod 16 counter JK flip flop
- 3. A sequential circuit with two D flip-flops A and B, one input x and one output z is specified by the following next-state and output equations:
- $A(t+1)=A^+B, B(t+1)=B^x, z=A+B^$
- (1) Draw the logic diagram of the circuit
- (2) Draw the state table
- (3) Draw the state diagram of the circuit
- (4) Characteristics table and excitation table
- 4. Consider the design of 4-bit BCD counter that counts in the following way 0000, 0010, 0011,..., 1001 and back to 0000
- (i) Draw the state diagram

UNIT-IV-PROCESSOR

Part A:

1. Define MIPS .

MIPS:One alternative to time as the metric is MIPS(Million Instruction Per Second)MIPS=Instruction count/(Execution time x1000000). This MIPS measurement is also called Native MIPS todistinguish it from some alternative definitions of MIPS.

2. Define MIPS Rate

The rate at which the instructions are executed at a given time.

3. Define a data path in a CPU.

A unit used to operate on or hold data within a processor. In the MIPS implementation, the data path elements include the instruction and data memories, the register file, the ALU, and adders.

4. Name the control signals required to perform arithmetic operations.

Reg Not (b) Reg write (c) ALL src (d) PCsrc (e) Mem Read (f) Mem to Reg

5. Define pipelining.

Pipelining is a technique of decomposing a sequential process into sub operations with each sub process being executed in a special dedicated segment that operates concurrently with all other segments.

6. Define parallel processing.

Parallel processing is a term used to denote a large class of techniques that are used to provide simultaneous data-processing tasks for the purpose of increasing the computational speed of a computer system. Instead of processing each instruction sequentially as in a conventional computer, a parallel processing system is able to perform concurrent data processing to achieve faster execution time.

7. What is meant by pipeline bubble?

Pipeline bubble or pipeline stall is a delay in execution of an instruction in an instruction pipeline in order to resolve the hazard. During the decoding stage, the control unit will determine if the decoded instruction reads from a register that the instruction currently in the

8. What is the ideal CPI of a pipelined processor?

The ideal CPI on a pipelined processor is almost always 1. Hence, we can compute the pipelined CPI:

9. Mention the various types of pipelining.

It is divided into 2 categories:

- □ Arithmetic Pipeline
- □ Instruction Pipeline

10. Mention the various phase in executing an instruction.

- □ Fetch
- □ Decode
- □ Execute
- □ Memory
- □ Write Back

11. Define instruction pipeline.

The transfer of instructions through various stages of the CPU instruction cycle.,including fetch opcode, decode opcode, compute operand addresses. Fetch operands, execute Instructions and store results. This amounts to realizing most (or) all of the CPU in the form of multifunction pipeline called an instruction pipelining

12. What are the advantages of pipelining?

The cycle time of the processor is reduced, thus increasing instruction issue rate in most cases. Some combinational circuits such as adders or multipliers can be made faster by adding more circuitry. If pipelining is used instead it can save circuitry and also a more complex combinational circuit.

13. What is meant by branch prediction?

Branch prediction, Predict the next fetch address. There are two branch prediction techniques:

- \Box Static branch prediction
- □ Dynamic branch prediction

The performance of branch prediction technique depends on

- □ Accuracy
- □ Cost

14. Give the features of the addressing modes suitable for pipelining.

The addressing modes used in modern processors often have the following features:

Access to an operand does not require more than one access to the memory

Only load and store instructions access memory

operands The addressing modes used do not have side effects

15. What is the role of cache memory in pipeline?

The use of cache memory is to solve the memory access problem. When cache is included in the processor the access time to the cache is usually the same time needed to perform other basic operation inside the processor.

16. Name the methods for generating the control signals.

The methods for generating the control signals are:

1) Hardwired control

2) Microprogrammed control

17. What are the two main approaches to hardware multithreading?

There are two main approaches to hardware multithreading. Fine-grained multithreading switches between threads on each instruction, resulting in interleaved execution of multiple threads. This interleaving is often done in a round-robin fashion, skipping any threads that are stalled at that clock cycle. Coarse-grained multithreading is an alternative to fine-grained multithreading. It switches threads only on costly stalls, such as last-level

cache misses.

18. State different types of hazards that can occur in pipeline.

The types of hazards that can occur in the pipelining were, 1. Data hazards. 2. Instruction hazards. 3. Structural hazards.

19. Define Data hazards

A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in pipeline. As a result some operation has to be delayed, and the pipeline stalls.

20. Define Instruction hazards

The pipeline may be stalled because of a delay in the availability of an instruction. For example, this may be a result of miss in cache, requiring the instruction to be fetched from the main memory. Such hazards are called as Instruction hazards or Control hazards.

21. Define Structural hazards?

The structural hazards is the situation when two instructions require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is access to memory.

22. What are the classification of data hazards?

Classification of data hazard: A pair of instructions can produce data hazard by referring reading or writing the same memory location. Assume that i is executed before J. So, the hazards can be classified as, 1. RAW hazard 2. WAW hazard 3. WAR hazard

23. Define RAW hazard :

(read after write) Instruction 'j' tries to read a source operand before instruction 'i' writes it.

24. Define WAW hazard :

(write after write) Instruction 'j' tries to write a source operand before instruction 'i' writes it.

25. Define WAR hazard :

(write after read) Instruction 'j' tries to write a source operand before instruction 'i' reads it.

26. List out the methods used to improve system performance. The methods used to improve system performance are 1. Processor clock 2.Basic Performance Equation 3.Pipelining 4.Clock rate 5.Instruction set 6.Compiler

Part B:

1. Draw and explain data path modified for pipelined execution

2. Explain various approaches used to deal with conditional branching.

3.Write in detail about the hardwired control.

- 4. Explain instruction pipelining.
- 5. What is branch hazard? Describe the method for dealing with the branch hazard?
- 6. What is data hazard? Explain the methods for dealing with data hazard?
- 7. Explain in detail about the designing of a control unit.

Part C:

Explain the basic concepts of pipelining and compare it with sequence processing with a

neat diagram GET

- 2. Explain different types of hazards that occur in a pipeline.
- 3. Explain in detail about the micro programmed control.
- 4. How to build a data path in ALU operations and in branch instructions

UNIT-5 MEMORY AND I/O

Part A:

1. What is meant by exception? Give one example of MIPS exception.

Exception is an unscheduled event that disrupts program execution; used to detect overflow. Or An exception or interrupt is essentially an unscheduled procedure call. The address of the instruction that overflowed is saved in a register, and the computer jumps to a predefined address to invoke the appropriate routine for that exception. The interrupted address is saved so that in some situations the program can continue after corrective code is executed. add S_1 , S_2 , S_1 ,

2. What is meant by address mapping?

Address mapping is defined as the smallest unit of addressed data that can be mapped independently in an area of the virtual address space.

3. Protein string matching code has four days execution time on current machinedoing integer instructions in 20 % of time, doing I/O in 35% of time and other operations in the remaining time. Which is the better trade off among the following two proposals? First: Compiler optimization that reduces number of integer instructions by 25% (assumeeach integer instruction takes the same amount of time); Second: Hardware optimization that reduces the latency of each I/O operations from 6µs to 5 µs. Solution:

4 days execution time on current machine 20% of time doing integer instructions

35% of time doing I/O Speed up integer ops X=0.2 S = (1/1-0.25)=1.33 $S_{int} = 1/(0.2/1.133+0.8) = 1.052$ Speed up IO X=0.35 $S = 6\mu s/5$ $\mu s = 1.2$ Speeding Up IO is better

Give example for each class in Flynn's classification.
SISD: Traditional Uniprocessor
SIMD: The intel Pentium 3
MISD: Multiple Frequency filters operating on a single signal stream
MIMD: Sun Ultra Services

5. Give the key characteristics of GPUs from CPUs:

- GPUs are accelerators that supplement a CPU, so they do not need be able to perform all the tasks of a CPU. This role allows them to dedicate all their resources to graphics. It's fine for GPUs to perform some tasks poorly or not at all, given that in a system with both a CPU and a GPU, the CPU can do them if needed.
- The GPU problems sizes are typically hundreds of megabytes to gigabytes, but not hundreds of gigabytes to terabytes.

6. What is Cluster?

Clusters are generally collections of computer connected to each other over their I/O interconnect via standard network switches and cables. Clusters are the best example of message passing parallel computer.

7. What are the three major distinctions Warehouse Scale computers have?

- \Box Ample, easy parallelism
- Operational Costs Count
- □ Scale and the Opportunities/Problems Associated with Scale

8. What are the classifications made by Flynn's?

The classifications defined by Flynn are based upon the number of concurrent instruction (or control) and data streams available in the architecture.

- 1. Single Instruction, Single Data stream (SISD)
- **2.** Single Instruction ,Multiple data stream(SIMD)
- **3.** Multiple Instruction, Single Data stream (MISD)

4. Multiple Instruction, Multiple Data streams

(MIMD) single program, multiple data (SPMD)

9. what is the basic philosophy of Vector Architecture?

The basic philosophy of vector architecture is to collect data elements from memory, put them in order

into a large set of registers, operate on them sequentially in registers using pipelined execution units,

and then write the results back to memory.

10. Define task level parallelism.

High performance can mean high throughput for independent task. Utilizing multiple processors by

running independent programs simultaneously is called as task level parallelism or process- level parallelism.

11. What are the various memory technologies?

- Main memory-SRAM semiconductor memory
- Main memory-DRAM semiconductor memory
- Flash semiconductor memory
- Magnetic disk

12. Define Hit Ratio.

Hit Ratio is the fraction memory access found in the upper level .It is often used as a measure of the performance of the memory hierarchy.

13. Distinguish SRAM and DRAM.

SRAMs are simply integrated circuits that are memory arrays with the single access port that can provide either read or a write. SRAMs have a fixed access time to any datum. SRAMs don't need to refresh and so the access time is very close to the cycle time. SRAMs typically use 6 to 8 transistors per bit to prevent the information from being disturbed when read. SRAM needs only minimal power to retain the charge in standby mode

In a DRAM the value kept in a cell is stored as a charge in a capacitor. A single transistor is then used to access this stored charge, either to read the value or to over write the charge stored there. Because DRAMs use only a single transistor per bit of storage, they are much denser and cheaper per bit than SRAM. As DRAM store charge on a capacitor, it cannot be kept indefinitely and must periodically be refreshed

14. What is virtual memory?

- □ A technique that uses main memory as a "cache" for secondary storage. Two major motive for Virtual Memory
- To allow efficiency and safe sharing of memory among multiple programs

□ To remove the programming burdens of a small, limited amount of main memory

15. Define memory hierarchy.

In computer architecture memory hierarchy is a concept used for storing and discussing performance issues in computer architectural design, algorithm predictions and the lower level programming constructs such as involving locality of reference. The memory hierarchy in computer storage distinguishes each level in the hierarchy by response time. Since response time, complexity and capacity are related, the levels may also be distinguished by their performance and controlling technologies.

16. State the advantages of virtual memory

- □ Easier memory management
- □ Provides memory isolation/ protection

17. What is cache memory?

Cache memory is random access memory (RAM) that a computer microprocessor can access more quickly that it can access regular RAMs

18. Define memory interleaving.

Memory Interleaving is a design made to compensate for the relatively slow speed of dynamic RAM by spreading memory address evenly across memory banks.

19. Summarize the sequence of the events involved in handling an interrupt request from a single device.

- The device raises an interrupt request
- The processor interrupts the program currently being executed
- Interrupts are disabled by changing the control bits in the PS
- The action requested by the interrupts is performed by ISR
- Interrupts are enabled and execution of the interrupted program is resumed

20. How many total bits are required for a direct map cache with 16KB of data and 4- word blocks, assuming a 32bit address?

Solution:

We know that 16KB is 4096, 4K words is 2^{12} words. Block size

of 4 words (2^2) , there are 1024 (2^{10}) blocks. Each block has 4 x

32 = 128 bits of data plus a tag.

Thus the total catch size is: $210 \times (128 + (32 - 10 - 2 - 2) + 1) = 210 \times 147 = 147$ bits

21. What is the use of DMA controller?

- Used for high speed I/O devices
- Device interface transfers data directly to or from the memory
- Processor not continuously involved

22. What is miss rate?

The miss rate (1-hit rate) is the fraction of memory accesses not found in the upper level.

23. State the advantages of the Virtual Memory.

- Virtual memory makes application programming easier by hiding <u>fragmentation</u> of physical memory.
- We can run more applications at once.

24. Specify the three types of the DMA transfer techniques?

- Single transfer mode (cyclestealing mode)
- Block Transfer Mode (Brust Mode)
- Demand Transfer Mode
- Cascade Mode

25. Why program controlled I/O is unsuitable for high-speed data transfer?

In program controlled i/o considerable overhead is incurred. Because several program instruction have to be executed for each data word transferred between the external devices and MM.Many high speed peripheral; devices have a synchronous modes of operation.that is data transfer are controlled by a clock of fixed frequency, independent of the cpu.

26. What are the steps taken when an interrupt occurs?

*Source of the interrupt

*The memory address of the required ISP

* The program counter &cpu information saved in subroutine

*Transfer control back to the interrupted program

27. Define interface.

The word interface refers to the boundary between two circuits or devices

28. What is programmed I/O?

Data transfer to and from peripherals may be handled using this mode. Programmed I/O

operations are the result of I/O instructions written in the computer program.

29. What is DMA?

A special control unit may be provided to enable transfer a block of data directly between an external device and memory without contiguous intervention by the CPU. This approach is called DMA

30. Differentiate Programmed I/O and Interrupt I/O

Sl. No	Programmed I/O	Interrupt I/O	
1 During polling processor is busy and therefore have serious and decremental effect on system throughput.		Here the processor is allowed to execute its instruction in sequence and only stop to service I/O device when it is told to do so by the device itself. This increase system throughput.	
2	It is implemented without interrupt hardware support	It is implemented using interrupt hardware support.	
3	It does not depend on interrupt status.	Interrupt must be enabled to process	
4	It does not need initialization of stack	It needs initialization of stack	



1. Explain in detail about the Von Neumann architecture.

2.List out the various addressing modes in detail and write a example for each.

3.Explain instruction set Architecture? Give examples.

Faculty Incharge

HoD











